Form PTO-1449 (modified)	Attorney Docket No. Intel 2207/12611	Serial No. 10/010,395
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT(S)' INFORMATION DISCLOSURE STATEMENT	Applicant Devadatta V. BODAS	
	Filing Date November 5, 2001	Group Art Unit 2183

U. S. PATENT DOCUMENTS

EXAMINER INITIAL	PATENT NUMBER	PATENT DATE	NAME	CLASS	SUBCLASS	FILING DATE*
TWC	5,761,456	June 2, 1998	Titus et al.	395	307	April 3, 1996
TWC	5,936,953	August 10, 1999	Simmons	370	364	December 18, 1997
TWC	6,304,930	October 16, 2001	Yamauchi	710	106	January 19, 1999

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
TWC	WO 00/58847	5 October 2000	WIPO	G06F	13/40	X	

OTHER DOCUMENTS

EXAMINER INITIAL	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
TWC	Luca Benini, Bologna, Italy; Giovanni DeMicheli, Stanford, CA, "System-Level Power Optimization: Techniques and Tools", 1999 International Symposium on Low Power Electronics and Design, (ISLPED), San Diego, CA., AUG. 16-17, 1999. International Symposium on Low Power Electronics and Design, New York, NY, ACM, 16 August 1999 (1999-08-16), 1-58113-133-X/99/0008, pages 288-293
TWC	L. Benini, Bologna, Italy; A. Bogliolo; G. DeMicheli, Stanford, CA, "System-Level Dynamic Power Management", Low-Power Design, 1999, Proceedings, IEEE Alessandro Volta Memorial Workshop on Como, Italy 4-5 March 1999, Los Alamitos, CA, USA, IEEE Comput. Soc., US, 4 March 1999 (1999-03-04), pages 23-31.
TWC	"Advanced Configuration and Power Interface Specification", Advanced Configuration and Power Interface Specification, XX, XX, Pages I-XII, 1-266.

EXAMINER	DATE CONSIDERED 8/23/04

EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.